



IC設計所

Institute of Integrated Circuit Design



SUSTAINABLE DEVELOPMENT GOALS

A Multi-Loop FVF Low-Dropout Regulator with Feed-Forward Ripple Cancellation

結合前饋式漣波抵銷之多重迴路 FVF 低壓差穩壓器

李沛錡 (Pei Chi Lee) | 指導教授 (Advisor): 王朝欽教授 (Prof. Chua-Chin Wang)

國立中山大學 電機工程學系 | Department of Electrical Engineering, National Sun Yat-sen University



Abstract

This work presents a fully integrated low-dropout regulator (LDO) in UMC 0.18- μm CMOS process that delivers 100 mA with a 342-pF on-chip output capacitor, a fast loop drives the PMOS pass transistor through a super source follower (SSF), and a slow loop with an error amplifier sets the DC accuracy.

To extend the power-supply rejection (PSRR) to 100 MHz, a current-mode feed-forward ripple cancellation (FFRC) circuit [1] senses the supply ripple through on-chip capacitors and injects a cancelling current into the SSF, so that the pass-transistor gate follows the supply. The injector also biases the SSF; no clock, comparator or digital calibration is needed.

Pre-layout simulations give a worst-case PSRR of **22.88 dB** from 100 kHz to 100 MHz over 17 loads (0–100 mA); at 100 mA the 100-MHz PSRR rises from 0.16 to **26.57 dB**.

A 0 $\leftrightarrow$ 100-mA step (100-ns edge) gives $-49.77 / +58.55$ mV.

Motivation & Goals

- Without an external μF capacitor, the PSRR of a fully integrated LDO collapses above a few MHz; surveyed designs with $I_{\text{max}} \geq 50$ mA reach only 0–30 dB at 10 MHz [2]–[5], and none reports 100 MHz.
- FVF LDOs respond fast and suit capacitor-less operation, but multi-loop FVF LDOs are mostly limited to 10–50 mA [7], [8].
- Goal:** single 1.8-V supply, 100 mA, no external components, PSRR ≥ 20 dB from 100 kHz to 100 MHz at every load from 0 to 100 mA.

22.88 dB

worst PSRR
100 kHz – 100 MHz

26.57 dB

PSRR @ 100 MHz
at $I_L = 100$ mA

100 mA

fully integrated
single 1.8-V supply

49.77 mV

undershoot 0 $\rightarrow$ 100 mA
100-ns edge

Circuit Architecture

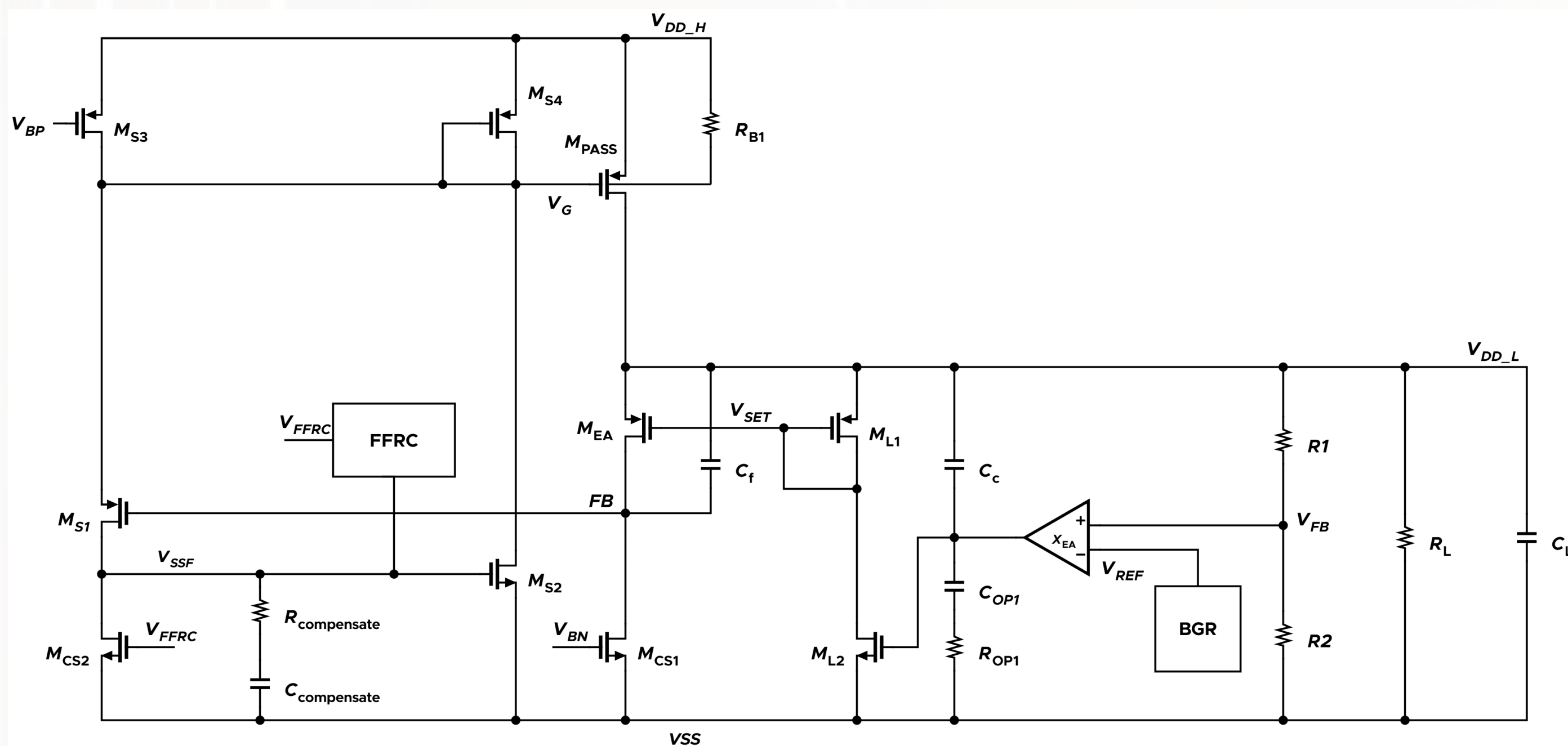


Fig. 1 Multi-loop FVF LDO

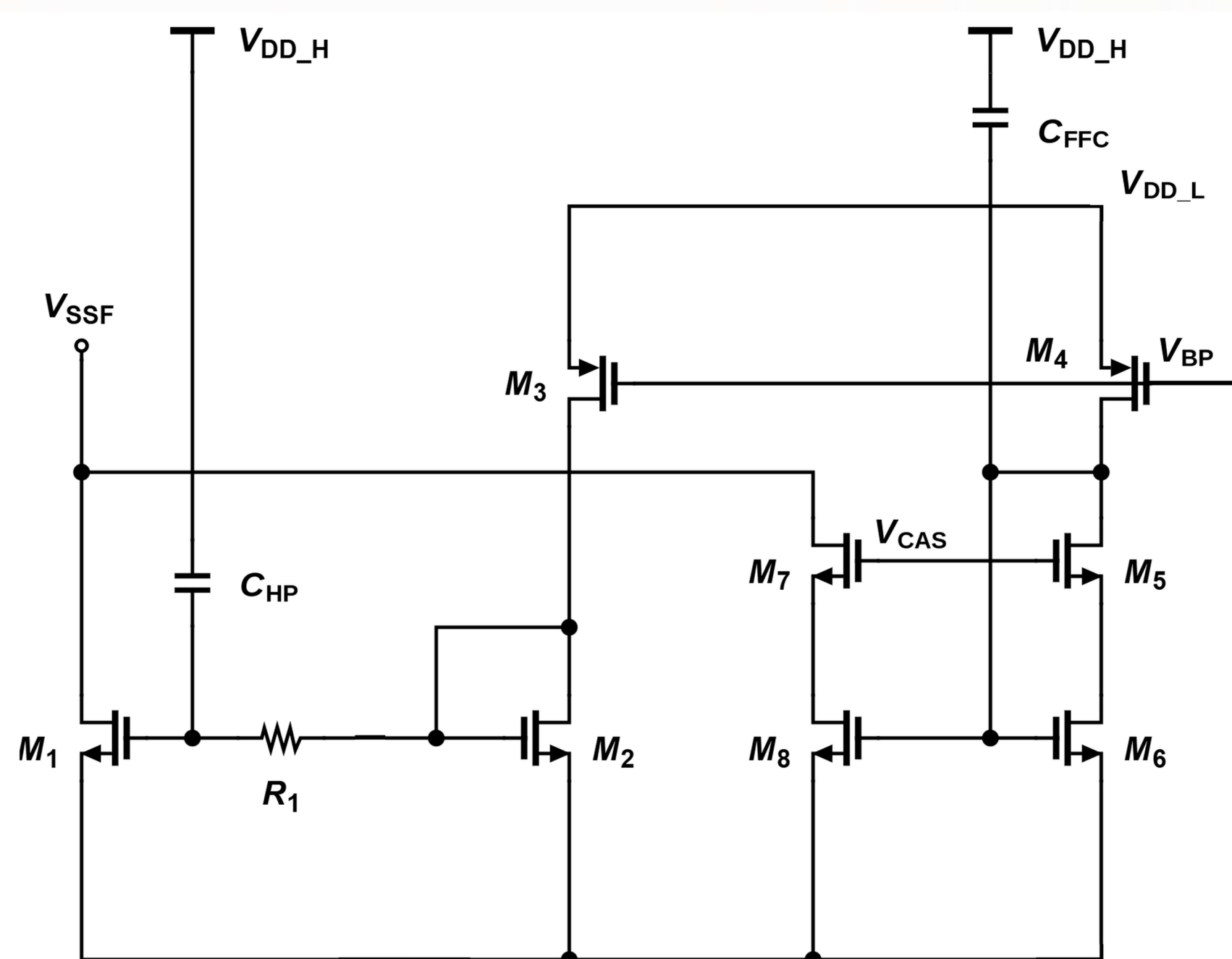


Fig. 2 FFRC injector (bias circuits omitted)

Simulation Results (pre-layout: TT, 27 °C, $V_{\text{IN}} = 1.8$ V, $V_{\text{OUT}} = 1.5$ V)

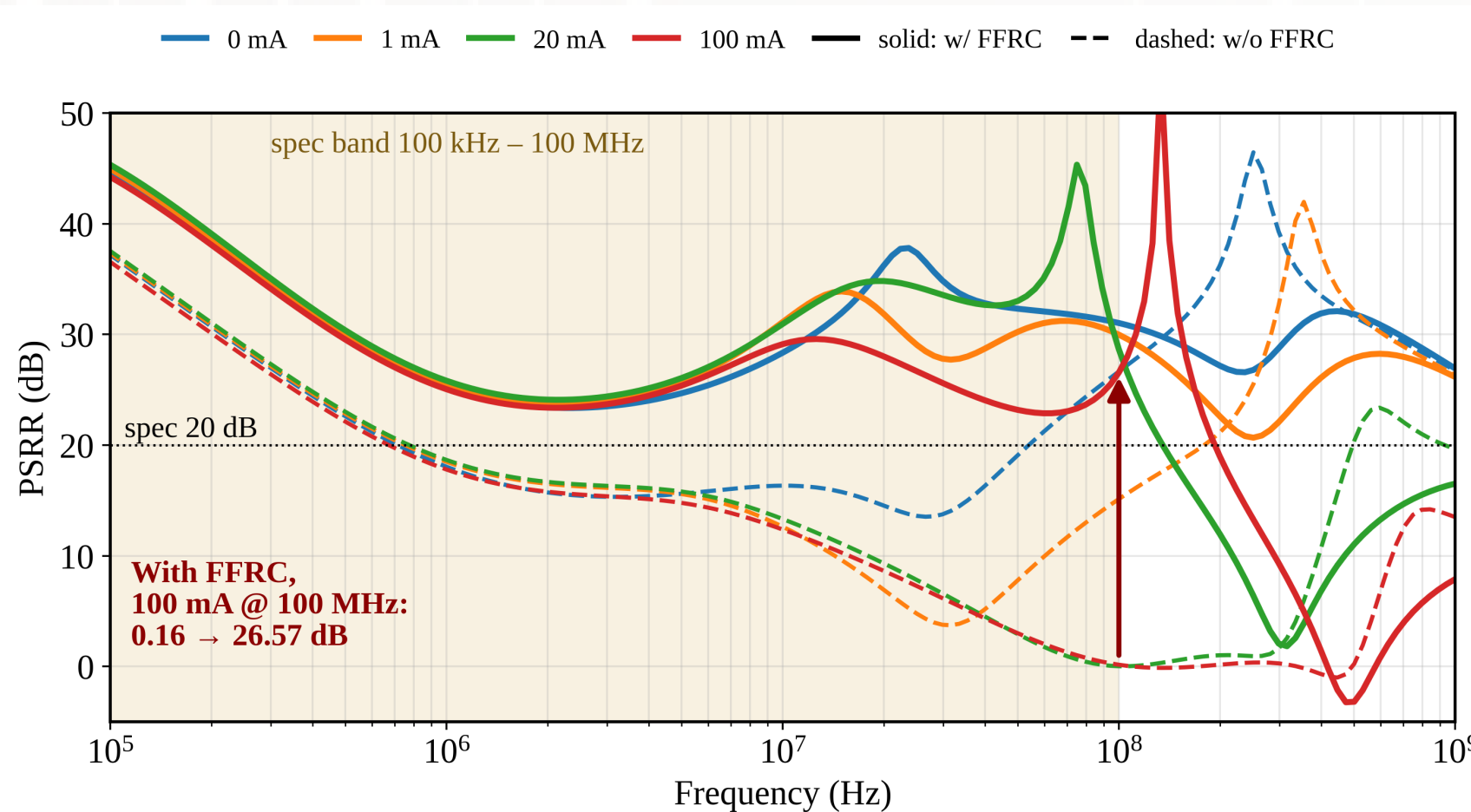


Fig. 3 PSRR without / with FFRC: worst 0.02 dB $\rightarrow$ 22.88 dB (17 loads, 100 kHz – 100 MHz).

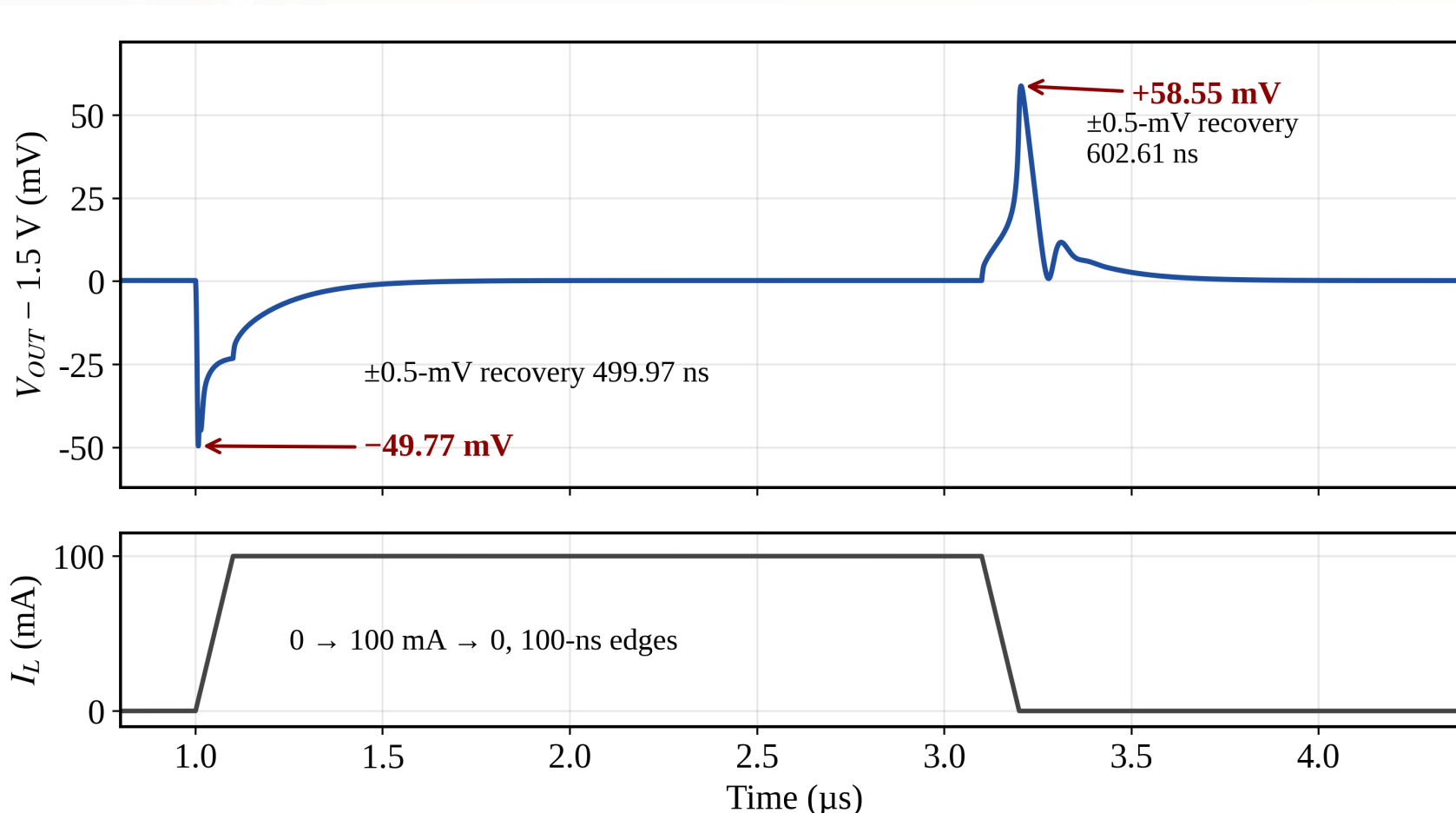


Fig. 4 Load transient 0 $\leftrightarrow$ 100 mA (100-ns edges): $-49.77 / +58.55$ mV, no ringing.

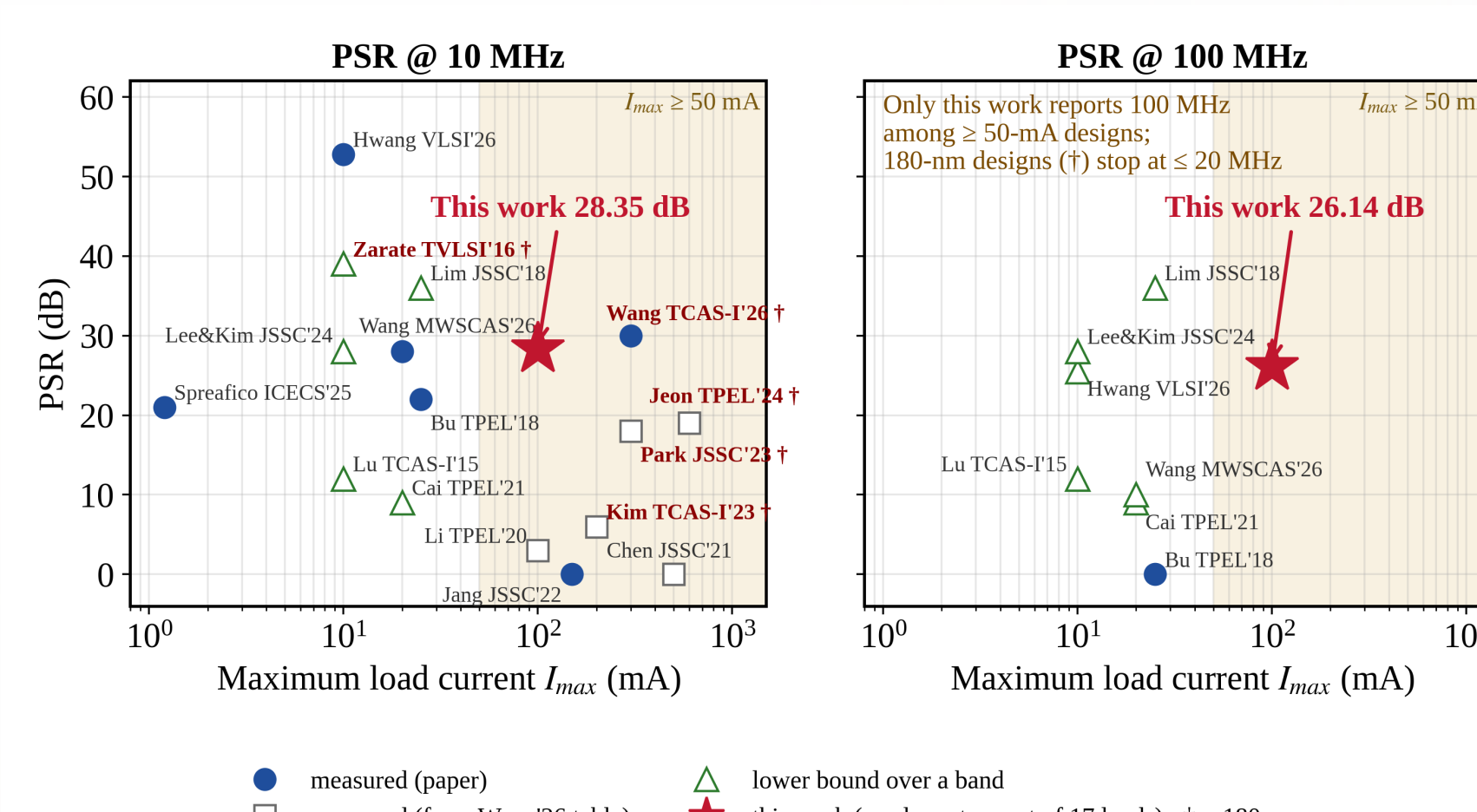


Fig. 5 Comparison: PSR at 10 / 100 MHz vs. I_{max} (papers: measured; this work: pre-layout simulation).

Performance Comparison

	This work	Wang TCAS-P'26 [2]	Jeon TPEL'24 [3]	Jang JSSC'22 [4]	Lee TPEL'25 [5]	Lim JSSC'18 [6]	Huang TPEL'19 [7]
Process	180 nm	180 nm	180 nm	28 nm	40 nm	65 nm	65 nm
Architecture	Multi-loop FVF + SSF + current-mode FFRC	Dual-loop + N-SSF	Multi-feedback loops	Time-domain (VTC + CP)	Segmented NMOS + active FFRC	Adaptive ripple cancellation	FVF + SSF
Pass device	PMOS	NMOS	NMOS	PMOS	NMOS	PMOS	PMOS
I_{max} (mA)	100	300	600	150	500	25	50
On-chip C_L (pF)	342	50	100	100	165	240	0 (external)
I_Q (μA)	695	58–118	27.5	31–110	300–350	154–298	50–190
PSR @ 1 MHz (dB)	25.05	44	40	≈ 20	44.6	≥ 36	n/r
PSR @ 10 MHz (dB)	28.35	30	19 †	≈ 0	n/r	≥ 36	n/r
PSR @ 100 MHz (dB)	26.14	n/r	n/r	n/r	n/r	≥ 36	n/r
PSR range reported	0.1–100 MHz 17 loads, 0–100 mA $-49.8 / +58.6$ mV 0 $\leftrightarrow$ 100 mA, 100 ns	up to 10 MHz	up to ≈ 20 MHz	> 10 MHz (PSR < 0 dB)	1 kHz – 10 MHz	10 kHz – 1 GHz	figure only
Load transient	$-49.8 / +58.6$ mV 0 $\leftrightarrow$ 100 mA, 100 ns	18 mV 1–272 mA, 100 ns	116 mV † 1–599 mA, 100 ns	–94 / +91 mV 1–149 mA, 40 ns	96 mV 5–305 mA, 10 ns	–225 / +153 mV 25 mA, 100 ns	–80 / +77 mV 0.1–50 mA, 2 ns
Clock / CP / digital	None	Gate-drive supply + comparators	2nd supply or CP	100-MHz clock	CP + comparators	None	None
Result	Pre-layout sim.	Measured	Measured	Measured	Measured	Measured	Measured

n/r: not reported; †: from the comparison table of [2]; PSR is given as rejection (positive dB). This work: worst of 17 loads (0–100 mA), pre-layout simulation, TT 27 °C; others: silicon measurements at the loads stated in each paper.

Conclusion

- A current-mode FFRC extends the PSRR of a 100-mA fully integrated FVF LDO to 100 MHz (worst 22.88 dB, 0–100 mA).
- The injector doubles as the SSF bias; single 1.8-V supply, no clock, comparator or digital calibration.
- Limitations: lower PSRR near 1 MHz and higher I_Q (SSF driver) than some prior art. Post-layout results will be shown at the exhibition.

References

- [1] K. Joshi et al., IEEE JSSC, vol. 55, no. 8, pp. 2151–2160, Aug. 2020.
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